**E0 217 Project Report (Aug 2023)**

**Project Title:** Design, Implementation and Simulation of an 8-point FFT Circuit in 45nm CMOS

**Names and IISc Email IDs of Group Members:**

|  |  |  |
| --- | --- | --- |
|  | Name | IISc Email ID |
| 1. |  |  |
| 2. |  |  |

**What are the contributions of each group member?**

|  |  |  |
| --- | --- | --- |
|  | Name | Contributions |
| 1. |  |  |
| 2. |  |  |

**What is the number of clock cycles required per FFT computation?**

**What is the area of the synthesized design?**

**What is the maximum clock frequency supported by the synthesized design?**

**What is the total power consumption of the synthesized design when operating at its maximum clock frequency? Provide breakdown of total power into leakage, switching and internal.**

**What is the total energy consumption of the synthesized design per FFT computation?**

**How does the total energy consumption of the synthesized design depend on the clock frequency?**

**What is the process corner, supply voltage and operating temperature at which the above metrics have been simulated?**

**What is the maximum absolute error when computing FFT of {0, 1, 2, 3, 4, 5, 6, 7}? Separately consider real and imaginary parts of each of the 8 outputs. Show calculations.**

**How can the FFT circuit be modified to compute Inverse FFT? Provide brief explanation only. No need to show any Verilog or simulation results.**

**Design Details:**

Provide detailed circuit diagrams and block diagrams. Explain all architectural trade-offs and other design parameters. Remember to cite all references.

**References:**

**Provide screenshots of all simulation, synthesis and analysis steps and tool runs.**

**Provide Verilog hardware descriptions of the FFT circuit design and the test bench.**